REMARKS/ARGUMENTS

Upon entry of this amendment, which amends claims 20 and 25, claims 20-25 remain pending. Support for all amended claims can be found in the specification, and no new matter has been added.

Claims 20-23 were rejected under 35 U.S.C. §102(e) as being anticipated by Senso et al., U.S. Patent No. 5,481,306. Claims 24 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Senso.

Reconsideration in view of the foregoing amendments and following remarks is respectfully requested.

Response to Examiner Inquiry Regarding the Lazar Paper

In the latest Office Action, the Examiner asked for clarification regarding inventorship in view of the paper by Paul Lazar et al. entitled "An Embedded Frame Buffer for Graphics Applications" ("the Lazar paper"), which constitutes Appendix A of the present application. The Examiner also requested clarification as to how the Lazar paper came to be included in the ultimate parent of the present application, which was filed before the Lazar paper was published.

In response, Applicant submits the attached declaration by Dr. Robert J. Proebsting, sole inventor of the present application. In view of Dr. Proebsting's statement, the following sequence of events can be established: Dr. Proebsting invented the subject matter claimed in the present application and subsequently disclosed it to Mr. Lazar and other co-workers at Hyundai Electronics America. Thereafter, Mr. Lazar and his co-authors wrote the Lazar paper, which describes a specific device that incorporates the claimed subject matter. A draft version of the Lazar paper was provided to Mr. Babak Sani, the attorney who prepared the ultimate parent of present application, and was filed therein as Appendix A in August 1996. Some months later (December 1996), the Lazar paper was published.

It is hoped that this information resolves the Examiner's question.

Response to Examiner Inquiry Regarding State of the Art

The Examiner also asked for clarification as to whether the concept that "neighboring arrays which shared sense amplifiers were not permitted to be open at the same time" was known in the art at the time of the invention.

Applicant believes that this question can best be answered by reference to U.S. Patents No. 6,026,044 and No. 6,031,783, to which the present application is related. Specifically, the '044 patent issued from Application No. 08/884,845 (grandparent of the present application), and the '783 patent issued from Application No. 09/179,260 (parent of the present application).

The '044 patent describes and claims, inter alia, a memory circuit with a plurality of arrays and a plurality of clusters of sense amplifiers, where each cluster has sense amplifier circuits coupled to columns in arrays on either side of the cluster. The memory circuit also includes array enable logic blocks, each of which is configured to activate an array and keep the array active until receiving "a subsequent row access command accessing a different row in that array, or a row in an adjacent array sharing a cluster of sense amplifiers." (See, e.g., claim 5 of the '044 patent.)

The '783 patent describes and claims, inter alia, a video chip with a memory circuit that has a plurality of arrays and a plurality of clusters of sense amplifiers, where each cluster has sense amplifier circuits coupled to columns in arrays on either side of the cluster. The memory circuit also includes array enable logic blocks, each of which is configured to activate an array and keep the array active until receiving "a subsequent row access command accessing a different row in that array, or a row in an adjacent array sharing a cluster of sense amplifiers." (See, e.g., claim 1 of the '783 patent).

Thus, it appears to Applicant that the Patent and Trademark Office has already acknowledged that a memory circuit having such features is Applicant's invention. It is hoped that this information will resolve the Examiner's question.

Erratum in "Notice of References Cited"

The "Notice of References Cited" (PTO-892) received with the latest Office Action appears to contain a typographical error. Specifically, the Notice cites US-5,877,789 but

the accompanying references included US-5,877,780 instead. Applicant notes that the '789 patent is in an unrelated art (ink-jet systems) and has therefore inferred that the Examiner intended to cite the '780 patent, which relates to memory circuits. Assuming that this inference is correct, Applicant respectfully requests the Examiner's assistance in correcting the Notice so that the '780 patent is properly included in the "References Cited" data when the present application issues.

Rejection of Claims 20-23 under 35 U.S.C. §102(e)

Independent claims 20 and its dependent claims 21-23 were rejected under 35 U.S.C. §102(e) as being anticipated by Senso et al., U.S. Patent No. 5,481,306. Applicant respectfully traverses.

Senso discloses a system for displaying a "Hi-Vision" (i.e., high-definition television, or HDTV) picture using a 3x4 array of NTSC-compliant receivers. The system divides the pixels of the HDTV picture into twelve blocks, each of which can be delivered to a different NTSC receiver (col. 3, lines 27-33; see also Fig. 2(c)). Vertical division is accomplished using six frame memories (FM1 to FM3 and FM1' to FM3' in Fig. 3), each of which stores roughly a third of the horizontal lines for one of the two fields of the (interlaced) HDTV picture (col. 4, lines 58-67). The lines are then read from the frame memories by three vertical filters VF1-VF3 that perform 5:7 scaling to increase the number of lines (col. 6, lines 23-29). In a "horizontal dividing portion (4)," the vertical filters VF1-VF3 divide each resulting line horizontally into four sections and store each section in a different "1H memory" H11 through H34 (col. 7, lines 31-37). These twelve memories are read out into twelve D/A converters DA11 through DA34 and recorded to video disks for playback by twelve NTSC devices (col. 7, lines 43-61).

The rejection identifies horizontal dividing portion 4, which stores lines of pixel data into the twelve 1H memories, as performing the claimed step of "storing data representing each of said plurality of pixel groups, respectively, in a row of a plurality of non-adjoining arrays in the memory circuit" as recited in claim 20. This is inaccurate for at least two reasons: (1) Senso fails to disclose or even suggest that 1H memories H11-H34 could correspond to "a

memory circuit that has a plurality of arrays wherein adjoining ones of the plurality of arrays share sense amplifiers" as recited in claim 20; and (2) even assuming memories H11-H34 could have such a structure, Senso fails to disclose or suggest that data for the pixel groups of one horizontal line could be stored in "a row of a plurality of non-adjoining arrays in the memory circuit."

First, as to the internal structure of the 1H memories, Senso discloses little. In particular, Senso does not disclose or suggest that any of the 1H memories H11-H34 includes a plurality of arrays, let alone that "adjoining ones of the plurality of arrays share a cluster of sense amplifiers," as recited in claim 20. Nor does Senso disclose or suggest that a group of 1H memories could be implemented using different arrays of a single memory circuit. Instead, Senso consistently describes the 1H memories H11-H34 as "twelve 1H memories" (see, e.g., col. 7, lines 43-46), suggesting twelve distinct memory circuits. Senso further discloses that:

> [e]ach of the 1H memories H11 through H34 includes two 1H memories so that the operation of writing the data into one 1H memory on the basis of the clock signal of the clock $\phi 4$ [for example 22.7 MHz; col. 6, line 9] and the operation of reading the data from the other 1H memory on the basis of the clock signal $\phi 5$ (for example, 5.67 MHz) are alternately performed. Col. 7, lines 37-42.

Since the two memories in, e.g., H11 are responsive to different clocks, it can be inferred that each of memories H11-H34 includes two separate memory circuits. Thus, as best understood, memories H11-H34 (or even just H11-H14) cannot correspond to different arrays of the same memory circuit. And even if such a correspondence could be inferred, Senso provides no disclosure or suggestion of how sense amplifiers in such a circuit might be arranged.

Second, even assuming arguendo that Senso could be read as suggesting that memories H11-H34 might be implemented as a memory circuit with a plurality of arrays, with adjoining arrays sharing clusters of sense amplifiers, the claimed step of storing data for one line in *rows in non-adjoining* arrays is not taught or suggested. Senso discloses that data for one line is stored in memories H11-H14 (or H21-H24 or H31-H34 depending on the vertical location of the line). If memories H11-H14 were implemented as arrays in one memory circuit, the natural ordering of the arrays would be H11, H12, H13, H14, and Senso suggests nothing to the

contrary. Thus, memories H11 and H12 (for instance), which store portions of the data for one line, would be adjoining arrays that share sense amplifiers, and the claimed step of storing pixel groups for one horizontal line "in a row of a plurality of *non-adjoining* arrays in the memory circuit" would not be met.

For at least these reasons, independent claim 20 is patentable over Senso, and claims 21-23, which depend from claim 20, derive patentability therefrom. Withdrawal of the rejection of claims 20-23 under 35 U.S.C. §102(e) is respectfully requested.

Rejection of Claims 24 and 25 under 35 U.S.C. §103(a)

Claims 24 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Senso. Applicant respectfully traverses.

The rejection asserts that Senso discloses a 3x4 division of a display panel and that it would have been obvious "to divide the display into halves or multiple variations, based upon the memories available/design choice (i.e. 2 memories/2 halves)." This represents a misunderstanding of Senso. Senso's 3x4 division is not related to any properties of memory devices; it is a consequence of the respective aspect ratios for HDTV and NTSC pictures (col. 3, lines 16-37). Thus, it is not clear to Applicant what motivation would exist to modify Senso to divide the picture into two halves as recited in claims 24 and 25.

But even if motivation for such a modification could be established, Senso still would not teach or suggest the claimed method because Senso does not disclose a memory circuit with arrays, some of which share sense amplifiers, or any order of storing data to arrays in a memory circuit.

With regard to independent claim 25, as discussed above, Senso does not teach or suggest that memories H11-H34 could be implemented as "a memory circuit that has a plurality of arrays wherein each odd numbered one of the plurality of arrays shares a cluster of sense amplifiers with an even numbered one of the plurality of arrays" as recited in claim 25. Instead, Senso plainly suggests that each of memories H11-H34 is itself comprised of two separate memory circuits.

Further, even assuming arguendo that memories H11-H34 could correspond to arrays of a memory circuit, Senso teaches that data would be stored to these arrays in sequential order, as discussed above. For instance, if memory H11 were an even array, memory H12 would be an odd array and so on, so that data for the first half would not be stored "in odd numbered arrays in the memory circuit" while data for the second half is stored "in even numbered arrays in the memory circuit" as claim 25 recites.

For at least these reasons, claim 25 is patentable over Senso. These arguments also apply with equal force to claim 24, which recites steps similar to those recited in claim 25, and claim 24 also derives patentability from its parent claim 20, which is patentable for at least the reasons discussed above.

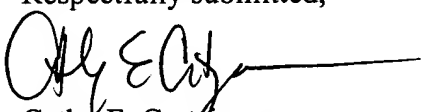
Withdrawal of the rejection of claims 24 and 25 under 35 U.S.C. §103(a) is respectfully requested.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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